Agilent E5910A
Serial Link Optimizer for Xilinx FPGAs

Data Sheet

Automatically tune your MGT-based serial links for optimal performance

Agilent Technologies and Xilinx have combined tools and technology to create a powerful test and analysis solution focused on the challenges of implementing high-speed serial links using Xilinx multi-gigabit transceivers (MGTs). The advanced technology of Xilinx MGTs gives you the flexibility to implement high-speed serial interfaces while enjoying the time-to-market advantages and flexibility that programmable devices offer. As you look to use serial interfaces in more of your designs, Agilent brings you the test and measurement capability you need to ensure a quality product that meets your time-to-market goals. The ability to quickly assess margin and automatically tune transmitter and receiver settings for optimal margin offers the potential to save you weeks of design time while improving your product's quality.

Test infrastructure based on internal BERT measurement

Agilent's E5910A serial link optimizer solution begins with Xilinx's ChipScope Pro Serial I/O Toolkit, which provides the infrastructure required to specify and implement a bit error ratio test (BERT) core that is placed in your FPGA. This internal BERT (IBERT) core provides the necessary functions to implement a BER test on the MGTs you specify, and it includes the ability to access the transmitter and receiver equalization settings in real-time. Using this IBERT core, Agilent's serial link optimizer software communicates with the core via JTAG (using the Xilinx cable) to make measurements and control the MGT transmitter and receiver settings.

This measurement system architecture (see Figure 1) requires no external hardware other than the standard Xilinx download cable, which minimizes your costs. Using an internal test core also allows you to measure post-equalization BER at the on-chip receiver input (as opposed to the pins of the device for a typical BER measurement). This approach means you can see the true effect of equalization settings on your link design and test and characterize its operation more reliably.

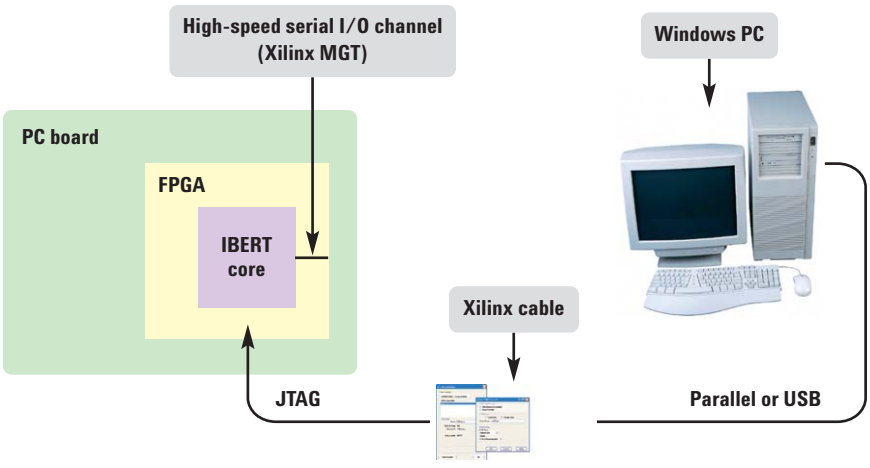

Figure 1. Block diagram of serial link optimizer measurement system

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Graphical environment simplifies setup and analysis

The serial link optimizer uses graphics extensively to simplify measurement setup and analysis. Its channel-oriented setup display occupies the left side of the application window and allows you to easily see the measurement configuration being used and make changes with simple pull-down and pop-up menus (see Figure 2). Controls are provided to let you specify transmitter and receiver selection and loopback mode, select line rate and test pattern, and access the transmitter and receiver settings that provide link tuning capability.

Measurements are the focus of the right side of the application window. Tabs are used to easily access the different measurement and analysis modes. In addition to basic BERT, the serial link optimizer provides graphical eye mapping capability for fast and simple interpretation of margin measurements. The Eye Map tab allows you to quickly create a representation of your link's eye opening to assess margin. The Tuning tab provides a simple eye map representation of the link's margin before and after tuning and gives you the ability to export the transmitter and receiver control settings after tuning via **Export Settings**. With this approach, you can quickly find the best equalization settings for your unique channel implementation and incorporate those settings into your design source.

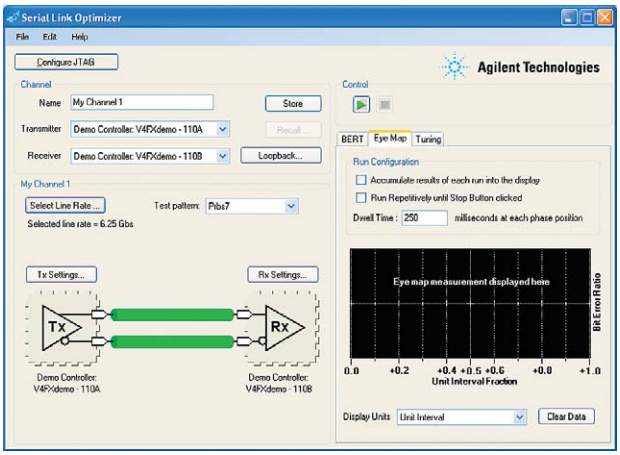

Figure 2. The serial link optimizer main window

A Quick Tour of the Application

Note: This quick tour assumes the implementation of the necessary IBERT core or cores has already taken place and the FPGA(s) has been programmed with the resulting bit files. For more information on this process, please consult Xilinx's ChipScope Pro Serial I/O Toolkit User Guide or the Agilent Serial Link Optimizer Design Guide.

Step 1

Configure serial link analyzer JTAG controllers

Use the Configure JTAG dialog box to specify the Xilinx cable or cables you will use to access the Xilinx FPGAs that implement the transmitter and receiver endpoints of your serial channel. The serial link optimizer supports up to two physical cable connections (one parallel plus one USB) and also supports remote cable connections.

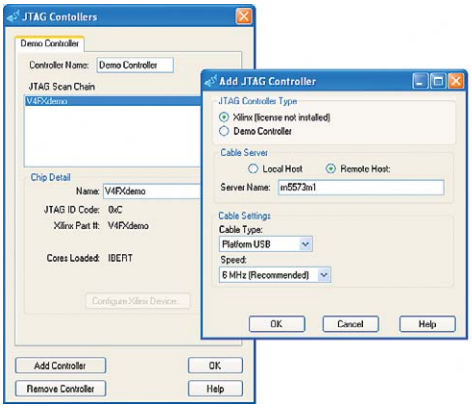

Figure 3. Add a JTAG controller for each Xilinx cable used

Step 2

Specify measurement setup

Use the menus to easily configure your channel measurement. Select the transmitter and receiver MGTs your design uses, specify the loopback configuration, set desired line rate according to your hardware design, and select the test pattern to be used by the serial link optimizer. If you want to manually adjust the transmitter and receiver control settings, click **Tx Settings** and **Rx Settings**.

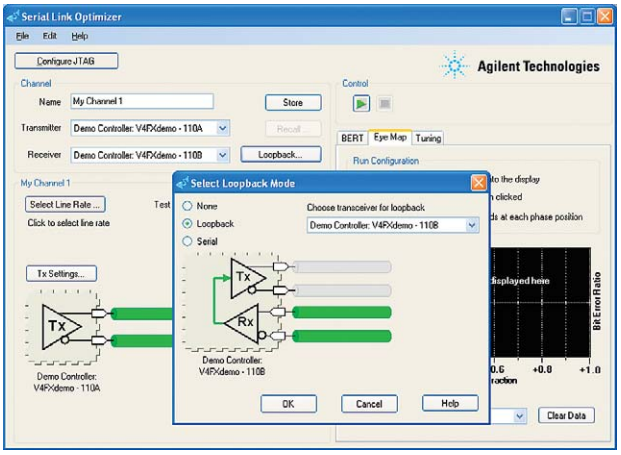

Figure 4. Select the loopback configuration with simple graphics

Step 3

Make measurements

Using the tabs for BERT, Eye Map, and Tuning, select your desired measurement, select any options with the radio buttons and press **[Run]**. It's that simple!

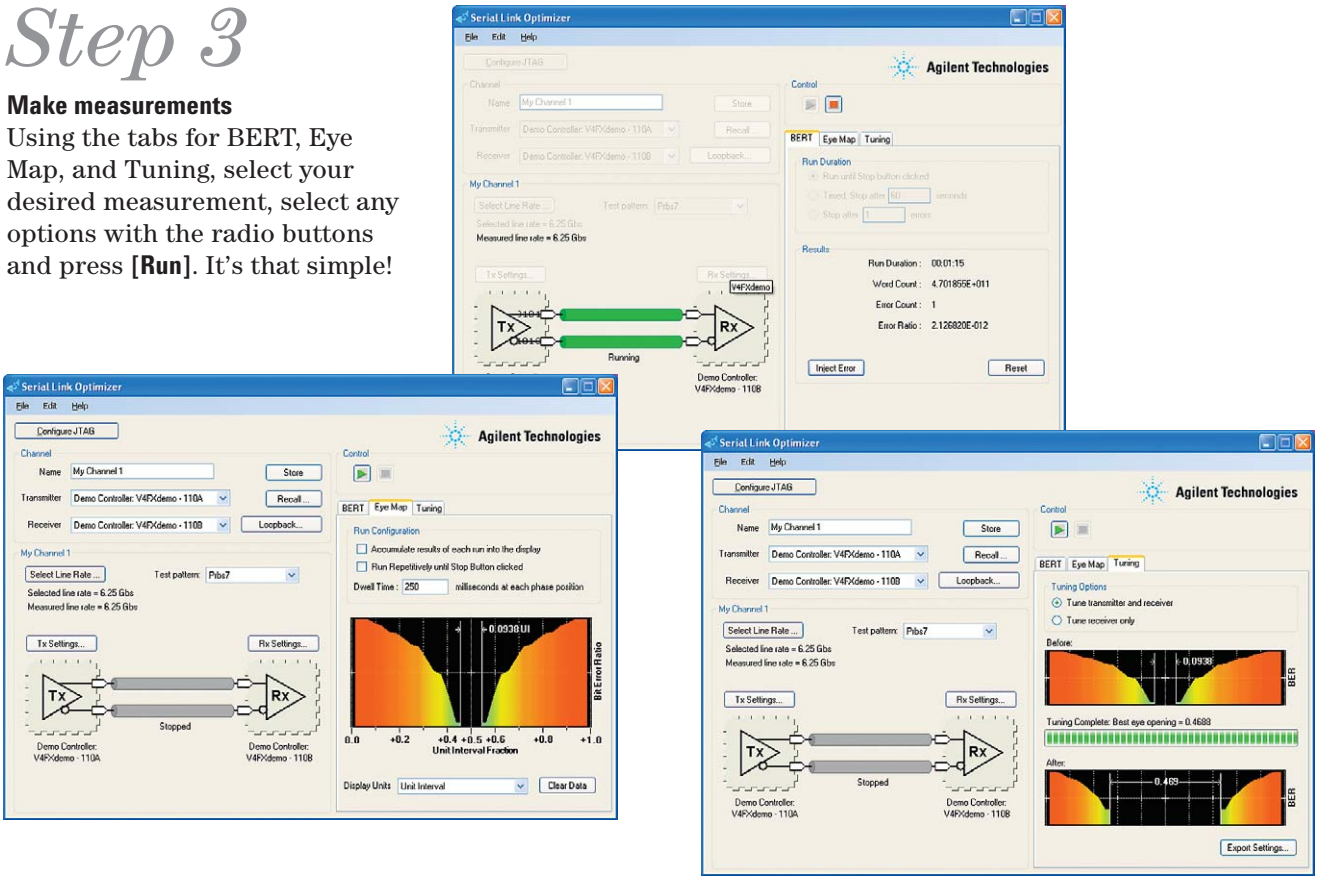

Figure 5. Tabs allow you to select BERT, Eye Map, or Tuning functions

Step 4

Export settings

After analysis and tuning, you may want to capture the MGT settings that result in the best margin for your circuit characteristics. Simply click **Export Settings** and a text (.txt) file is produced with the settings represented in Verilog, VHDL, and .ucf formats. You can then simply "cut and paste" the appropriate section back into your design source file to incorporate the tuned settings.

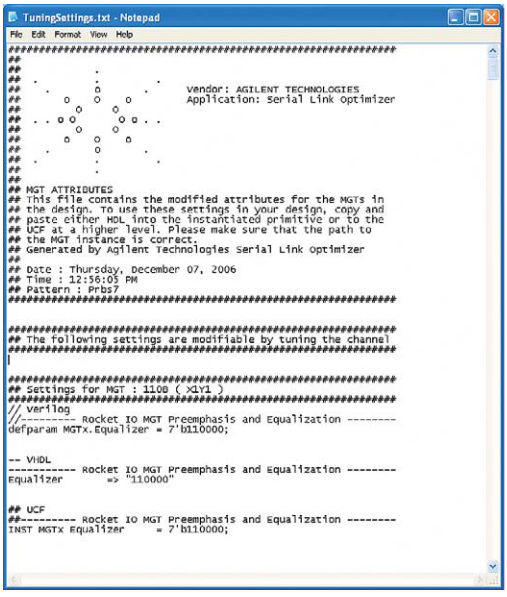

Figure 6. Export tuned MGT transmitter and receiver settings

E5910A serial link optimizer specifications and characteristics

Supported Xilinx FPGAs	Virtex-4 FX devices, Virtex-5 LXT and SXT support available in early 2007
Supported Xilinx programming cables (required)	Xilinx platform USB cable, parallel cable 3 and 4
Supported operating systems	Windows XP SP2 or higher
Compatible design tools	Xilinx ChipScope Pro Serial I/O Toolkit, version 9.1i or higher (required for IBERT core)

Ordering information

The Agilent E5910A serial link optimizer includes	CD with application software (optional – the latest software version may be downloaded from **www.agilent.com/find/fpga**)
Option 010	Entitlement certificate for 1-year node locked license
Option 011	Entitlement certificate for 1-year node locked license renewal
Option 020	Entitlement certificate for 1-year floating (server) license
Option 021	Entitlement certificate for 1-year floating (server) license renewal

Agilent E5910A serial link optimizer can be purchased from Xilinx Worldwide Distributors Avnet and Nu Horizons or your Agilent representative.

Related literature

Publication title	Publication type	Publication number
Agilent Serial Link Optimizer Design Guide	Technical Overview	5989-6048EN

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